IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
David Jia Chen et al.)
Serial No.: 10/665,654)
Group Art Unit: 2816)
Filed: September 18, 2003)
Examiner: Linh M. Nguyen)
For: *ELECTRONIC DELAY ELEMENT*)
)

APPEAL BRIEF

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Sir:

This Appellants' Appeal Brief is filed in response to a Final Office Action dated October 17, 2005 and a Notice Of Panel Decision From Pre-Appeal Brief Review dated April 3, 2006. Reconsideration of the Application, withdrawal of the rejections, and allowance of the claims are respectfully requested.

CERTIFICATE OF MAILING/FACSIMILE

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ON: September 10, 2007 (DATE) BY: Karen Taragowski Signature: /Karen Taragowski/ (Applicant, Assignee or Representative)

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines (IBM) of Armonk, NY.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-14 are pending.

Claims 1 through 14 are rejected.

The Appellants are appealing the rejection of independent claims 1, 9, 10, and 11 (all other remaining claims depend from these claims). Claims 1, 9, 10, and 1 are on appeal.

IV. STATUS OF AMENDMENTS

The Examiner issued a final rejection of claims 1-14 in the Final Office Action of October 17, 2005. Appellants submitted a Notice Of Appeal with a Pre-Appeal Brief Request For Review on January 17, 2006. The Notice Of Panel Decision From Pre-Appeal Brief Review dated April 3, 2006 indicated that a pre-appeal brief conference was held wherein the panel has determined that claims 1-14 are rejected. The application remains under appeal because there is at least one actual issue for appeal.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

This summary references line numbers of the specification as filed. It is to be noted that the text of each page of the filed specification starts with line number 5.

Independent claim 1 sets forth the following subject matter.

A) an input signal to be delayed; and: FIG. 3: reference 102; Specification at page 4, line 5; page 6, line 12; and Abstract line 2.

B) a series of at least two delay stages;: FIG. 3: references 301, 303, 305, 307, 309, 312, 315; Specification at page 4, line 5; page 5, lines 24-29.

C) wherein each of the delay stages includes a stack of uniform channel length transistors: FIG. 3; Specification at page 3, lines 26-29; page 4, lines 5-6; page 6, lines 1-13; and Abstract, line 5.

D) with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type: FIG. 3; Specification at page 5, lines 14-23.

E) without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other memory circuits on a chip;: FIG. 3; Specification at page 3, lines 26-29; page 5, lines 1-9; and Abstract, lines 5-7.

F) wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip;: Specification at page 3, lines 24-26; page 5, lines 6-8; page 6, lines 4-7; and Abstract, lines 5-7.

G) wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;: FIG. 3; Specification at page 4, lines 7-9; page 6, lines 10-13, 16-19, 22-25, 28-29 to page 7, lines 1-2; page 7, lines 7-12, lines 5-8, lines 11-14, lines 17-20, lines 23-26.

H) wherein a source of a top transistor in the stack is coupled to a first reference voltage;: FIG. 3; Specification at page 5, lines 18-20.

I) wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;: FIG. 3; Specification at page 5, lines 18-20.

J) wherein a drain of the top transistor is electrically coupled to a of the drain bottom transistor in the stage so as to form an output of the stage;: FIG. 4; Specification at page 4, lines 11-13.

K) wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and: FIG. 3; Specification at page 5, lines 22-24; page 6, lines 1-9; page 7, lines 1-26.

L) wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.: FIG. 3; Specification at page 5, lines 22-24; page 6, lines 1-9; page 7, lines 1-26.

Independent claim 9 sets forth the following subject matter.

A) at least one delay element; wherein the delay element includes: FIG. 3: reference 300;: Specification at page 3, line 25; page 4, line 4; page 5, line 6, lines 24-25.

B) an input signal to be delayed; and: FIG. 3: reference 102; Specification at page 4, line 5; page 6, line 12; and Abstract line 2.

C) a series of at least two delay stages;: FIG. 3: references 301, 303, 305, 307, 309, 312, 315; Specification at page 4, line 5; page 5, lines 24-29.

D) wherein each of the delay stages includes a stack of uniform channel length transistors: FIG. 3; Specification at page 3, lines 26-29; page 4, lines 5-6; page 6, lines 1-13; and Abstract, line 5.

E) with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type: FIG. 3; Specification at page 5, lines 14-23.

F) without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;: FIG. 3; Specification at page 3, lines 26-29; page 5, lines 1-9; and Abstract, lines 5-7.

G) wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other memory circuits;: Specification at page 3, lines 24-26; page 5, lines 6-8; page 6, lines 4-7; and Abstract, lines 5-7.

H) wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;: FIG. 3; Specification at page 4, lines 7-9; page 6, lines 10-13, 16-19, 22-25, 28-29 to page 7, lines 1-2; page 7, lines 7-12, lines 5-8, lines 11-14, lines 17-20, lines 23-26.

I) wherein a source of a top transistor in the stack is coupled to a first reference voltage;: FIG. 3; Specification at page 5, lines 18-20.

J) wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;: FIG. 3; Specification at page 5, lines 18-20.

K) wherein a drain of the top transistor is electrically coupled to a of the drain bottom transistor in the stage so as to form an output of the stage;: FIG. 4; Specification at page 4, lines 11-13.

L) wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and: FIG. 3; Specification at page 5, lines 22-24; page 6, lines 1-9; page 7, lines 1-26.

M) wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.: FIG. 3; Specification at page 5, lines 22-24; page 6, lines 1-9; page 7, lines 1-26.

Independent claim 10 sets forth the following subject matter.

A) at least one delay element; wherein the delay element includes: FIG. 3: reference 300; Specification at page 3, line 25; page 4, line 4; page 5, line 6, lines 24-25.

B) an input signal to be delayed; and: FIG. 3: reference 102; Specification at page 4, line 5; page 6, line 12; and Abstract line 2.

C) a series of at least two delay stages;L FIG. 3: references 301, 303, 305, 307, 309, 312, 315; Specification at page 4, line 5; page 5, lines 24-29.

D) wherein each of the delay stages includes a stack of uniform channel length transistors: FIG. 3; Specification at page 3, lines 26-29; page 4, lines 5-6; page 6, lines 1-13; and Abstract, line 5.

E) with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type: FIG. 3; Specification at page 5, lines 14-23.

F) without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other clock circuits on a chip;: FIG. 3; Specification at page 3, lines 26-29; page 5, lines 1-9; and Abstract, lines 5-7.

G) wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other clock circuits;: Specification at page 3, lines 24-26; page 5, lines 6-8; page 6, lines 4-7; and Abstract, lines 5-7.

H) wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;: FIG. 3; Specification at page 4, lines 7-9; page 6, lines 10-13, 16-19, 22-25, 28-29 to page 7, lines 1-2; page 7, lines 7-12, lines 5-8, lines 11-14, lines 17-20, lines 23-26.

I) wherein a source of a top transistor in the stack is coupled to a first reference voltage;: FIG. 3; Specification at page 5, lines 18-20.

J) wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;: FIG. 3; Specification at page 5, lines 18-20.

K) wherein a drain of the top transistor is electrically coupled to a of the drain bottom transistor in the stage so as to form an output of the stage;: FIG. 4; Specification at page 4, lines 11-13.

L) wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and: FIG. 3; Specification at page 5, lines 22-24; page 6, lines 1-9; page 7, lines 1-26.

M) wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.: FIG. 3; Specification at page 5, lines 22-24; page 6, lines 1-9; page 7, lines 1-26.

Independent claim 11 sets forth the following subject matter.

A) a first transistor with a source electrically coupled to a first reference voltage;: FIG. 3: reference 302; Specification at page 5, lines 18-19.

B) a last transistor with a source electrically coupled to a second reference voltage;: FIG. 3: reference 316; Specification at page 5, lines 18-19.

C) a totem pole of at least two transistors, the totem pole including:: FIG. 3; Specification at page 6, lines 1-2. T

D) a top transistor with a source electrically coupled to a drain of the first transistor;: FIG 3; Specification at page 3, lines 11-13; page 5, lines 16-23.

E) a bottom transistor with a source electrically coupled to a drain of the last transistor;: and FIG. 3; Specification at page 5, lines 16-23.

F) at least two transistors, wherein the transistors complete the totem pole arrangement: FIG. 3; Specification at page 6, lines 1-2.

G) wherein a drain of each of the transistors is electrically coupled to a source of an adjacent transistor within the transistors relative to the each of the transistors: FIG. 3; Specification page 4, lines 9-13.

H) and wherein each of the transistors within the totem pole comprise a uniform channel length transistor with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type: FIG. 3; Specification at page 5, lines 14-23

I) without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other delay circuits on a chip,: FIG. 3; Specification at page 3, lines 26-29; page 5, lines 1-9; and Abstract, lines 5-7.

J) the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other delay circuits;: Specification at page 3, lines 24-26; page 5, lines 6-8; page 6, lines 4-7; and Abstract, lines 5-7.

K) an input electrically coupled to each gate within the totem pole; and: FIG. 3; Specification at page 4, lines 7-9; page 6, lines 10-13, 16-19, 22-25, 28-29 to

page 7, lines 1-2; page 7, lines 7-12, lines 5-8, lines 11-14, lines 17-20, lines 23-26.

L) an output electrically coupled to connection between one source and one drain of two transistors within the totem pole;: FIG. 3; Specification at page 4, lines 11-13.

M) wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and: FIG. 3; Specification at page 5, lines 22-24; page 6, lines 1-9; page 7, lines 1-26.

N) wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.: FIG. 3; Specification at page 5, lines 22-24; page 6, lines 1-9; page 7, lines 1-26.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 9, 10, and 11 are unpatentable under 35 U.S.C. §102(b) as being anticipated by Sato et al. (U.S. Patent No 5,602,798).

VII. ARGUMENT

A. WHETHER CLAIMS 1, 9, 10, and 11 ARE ANTICIPATED BY SATO ET AL.

In the Examiner's Office Action of October 17, 2005, the Examiner rejected claims 1-14 under 35 U.S.C. §102(b) as being anticipated by Sato et al. (U.S. Patent No 5,602,798), hereinafter referred to as "Sato". The Appellants respectfully submit that claims 1-14 are patentable over Sato under 35 U.S.C. §

102(b). The Appellants assert that Sato does not teach, suggest, or anticipate the claimed limitations, particularly the claim limitations of:

> "wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;
>
> wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip" ...

Appellants respectfully suggest selection of independent claim 1 as representative of the independent claims on appeal. Independent claim 1 is directed towards a delay element, comprising:

an input signal to be delayed; and

a series of at least two delay stages;

wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;

wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip;

wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;

wherein a source of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;

wherein a drain of the top transistor is electrically coupled to a of the drain bottom transistor in the stage so as to form an output of the stage;

wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

The Appellants assert that, in particular, the underlined portions of the above claims are not taught or suggested by Sato.

The claims were rejected under 35 U.S.C. §102(b). The Statute expressly requires and a proper rejection requires that a single reference teach (i.e., identically describe) each and every element of the rejected claims as being anticipated by Sato.[1] As discussed below, the Appellants assert that these limitations, especially when considered in the context of the other limitations of claim 1, are not described in the prior art references of record and that these limitations render the claimed subject matter unobvious over the prior art.

Overview of Prior Art

The emphasis of Sato is a synchronous semiconductor memory device that is operable in a snooze mode. See Sato Abstract and col. 2, lines 61-67 to col. 3, lines 1-17. FIG. 14A of Sato discloses a delay element used in an internal snooze mode signal generating portion. See Sato col. 13, lines 14-34 and col. 14, lines 32-33. Sato discloses that the gate circuits of the delay element have the same structure and each include a plurality of (three) p-channel MOS transistors and a plurality of (three) n-channel MOS transistors. The gates of a plurality of MOS transistors are connected to an input node and the gate

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[1] See MPEP §2131 (Emphasis Added) "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim."

capacitances of these transistors, in combination, increase the capacitance of the input node. The p-channel MOS transistors are connected in series between a power supply node and an output node. Consequently, a resistance between the power supply node and output node increases so that a capability of supplying a current to the output node decreases, resulting in a slow rising of its potential.

Sato Fails to Describe All Limitations

With regards to claim 1, the Appellants traverse the Examiner's assertion that Sato discloses "wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip".

The Examiner, in the Final Office Action, cites Sato at col. 14, lines 35-36 in support of the assertion that Sato teaches "each of the delay stages includes a stack of uniform channel length transistors", as recited for the presently claimed invention. However, Sato merely states at col. 14, lines 35-36 that "[g]ate circuits 60a-60n have the same structure". The term "same structure" has more than one connotation, i.e., each of the gate circuits 60a-60n have the same number of transistors, the same layout of transistors, the same type of transistors, and more. Sato generally teaches "structure" without further defining what is meant by the term "structure". However, even arguendo, if the term "same structure" is used to connote "uniform channel length", as suggested by the Examiner, Sato is completely silent on how the gate circuits in the delay element relate to transistors in circuits outside the delay element. The term channel length, as known to one of ordinary skill in the art, is the distance between the source and drain of a transistor. Sato is silent on "wherein the use of uniform channel length

transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". The Appellants respectfully contend that "the same structure" as taught by Sato is not the same as "...uniform channel length transistors".

Furthermore, Sato teaches that in the delay element, all the gate circuits have the same structure, i.e., a gate circuit 60a has the same structure as any other gate circuit in the delay element 45aa. The presently claimed invention, on the other hand, recites "wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". Sato never mentions the channel length of a transistor and is completely silent on "each of the delay stages includes a stack of uniform channel length transistors". Sato teaches delay elements having gate circuits that have the same structure. There is no teaching that the "channel length" of the gate circuits are identical to channel length of other transistors outside the delay element "so that tolerances across the delay stages track tolerance of other circuits on a chip" and "wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip".

Stated differently, Sato is concerned with circuits only in the delay elements. The presently claimed invention, on the other hand, is directed towards a delay element that does not use extended channel length transistors, but includes uniform channel length transistors, so that "that tolerances across the delay stages track tolerance of other circuits on a chip". Sato is completely silent on "without using extended channel length transistors in the delay stages", as recited for the presently claimed invention. In fact, Sato never explicitly states or implies that extended channel length transistors are not used. Furthermore, nowhere does Sato teach uniform channel length transistors are used so that

"that tolerances across the delay stages track tolerance of other circuits on a chip". In other words, in the present invention the use of uniform channel length transistors allow for the tolerances across the delay stages to track other circuits on the chip and not just the delay element. The Appellants respectfully suggest that the Examiner is improperly interpreting the claim to recite that uniform channel length transistors are included in a delay stage so that tolerances can be track only across delay stages in a delay element and not "across other circuits in the chip".

Sato never teaches tracking tolerances. Even assuming arguendo that "same structure" in Sato is analogous to uniform channel length transistors, which it is not, Sato never teaches that the "same structure" allows for having tolerances for gate circuits in the delay stage track other tolerances across other circuits (e.g. other circuits besides that particular delay element) on the chip. Sato is only concerned with a single delay element and the gate circuits within that delay element.

Moreover, nowhere does Sato teach or suggest "the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip". Sato is directed towards the post-production stage of the circuit and is not concerned with providing uniform tolerance variations a circuit across a circuit during production. A post-production stage such as manufacturing/yield is not the same as parametric tracking. Yield is one measurement among several of the efficiency in a chip manufacturing process. Manufacturing yield is a reflection of the quality of the manufacturing process and drives cost. The presently claimed invention, on the other hand, is concerned with the manufacturing process, which naturally varies from wafer to wafer, by using parametric tracking. Designs that use a mixture of channel lengths result in non-uniform tolerance variations across the chip. Accordingly, the present invention distinguishes over Sato for this reason as well.

Accordingly, independent claims 1, 9, 10, and 11 distinguish over Sato for at least the reasons stated above. Claims 2-8, and 12-14 depend from claims 1 and 11 respectively. Since dependent claims contain all the limitations of the independent claims, claims 2-8, and 12-14 distinguish over Sato as well. Therefore, the rejection of claims 1-14 should be reversed.

CONCLUSION

For the reasons stated above, Appellants respectfully contend that each claim is patentable. Therefore, reversal of all rejections is courteously solicited.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. A delay element, comprising:

an input signal to be delayed; and

a series of at least two delay stages;

wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;

wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip;

wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;

wherein a source of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;

wherein a drain of the top transistor is electrically coupled to a of the drain bottom transistor in the stage so as to form an output of the stage;

wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

2. The delay element according to claim 1, wherein each stack of transistors includes additional transistors electrically coupled with the top transistor and the bottom transistor;

wherein a drain of a first additional transistor is electrically coupled to a source of the top transistor, a drain of the last additional transistor is connected to a source of the bottom transistor; and

wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack.

3. The delay element according to claim 1, wherein each transistor of the second conductivity type is a n-channel FET.

4. The delay element according to claim 1, wherein each transistor of the first conductivity type is a p-channel FET.

5. The delay element according to claim 2, wherein each transistor of the second conductivity type is a n-channel FET.

6. The delay element according to claim 2, wherein each transistor of the first conductivity type is a p-channel FET.

7. The delay element according to claim 1, wherein the input signal to be delayed is a clock signal.

8. The delay element according to claim 2, wherein the input signal to be delayed is a clock sign.

9. A memory circuit comprising:

at least one delay element; wherein the delay element includes:

an input signal to be delayed; and

a series of at least two delay stages;

wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other memory circuits on a chip;

wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other memory circuits;

wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;

wherein a source of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;

wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage;

wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

10. A clock circuit comprising:

at least one delay element, wherein each delay element includes:

an input signal to be delayed; and

a series of at least two delay stages;

wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other clock circuits on a chip;

wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other clock circuits;

wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;

wherein a source of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;

wherein a drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage;

wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

11. A delay circuit comprising at least one stack of transistors, each of the at least one stack of transistors comprising:

a first transistor with a source electrically coupled to a first reference voltage;

a last transistor with a source electrically coupled to a second reference voltage;

a totem pole of at least two transistors, the totem pole including:

a top transistor with a source electrically coupled to a drain of the first transistor;

a bottom transistor with a source electrically coupled to a drain of the last transistor; and

at least two transistors, wherein the transistors complete the totem pole arrangement, wherein a drain of each of the transistors is electrically coupled to a source of an adjacent transistor within the transistors relative to the each of the transistors, and wherein each of the transistors within the totem pole comprise a uniform channel length transistor with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other delay circuits on a chip, the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other delay circuits;

an input electrically coupled to each gate within the totem pole; and

an output electrically coupled to connection between one source and one drain of two transistors within the totem pole;

wherein when the input is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and

wherein when the input to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

12. The delay circuit according to claim 11, wherein each transistor of the first conductivity type is a p-channel FET.

13. The delay circuit according to claim 11, wherein each transistor of the second conductivity type is a n-channel FET.

14. The delay circuit according to claim 11, wherein the input signal to be delayed is a clock signal.

IX. EVIDENCE APPENDIX

NONE

X. RELATED PROCEEDINGS APPENDIX

NONE